UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/740,901	12/21/2000	Makoto Kidera	200901US2	6368

22850 7590 05/17/2004

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
HOGAN, MARY C	

ART UNIT	PAPER NUMBER
2123	5

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/740,901	KIDERA ET AL.
	Examiner	Art Unit
	Mary C Hogan	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/16/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/21/00* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application has been examined.

2. **Claims 1-9** have been examined and rejected.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file, specifically, Japanese Patent Application Number 222025/2000, filed on 07/24/2000.

Specification

4. The disclosure is objected to because of the following. Appropriate correction is required.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. A suggested title is: "Method for Simulating Variations In Device Parameters Resulting from Semiconductor Manufacture".

6. Page 6, line 5: the phrase "varying depending on variations" makes the sentence unclear in it's meaning.

Drawings

7. Figures 7-11 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. Figures 7-10 are described in the "Description of Background Art" which implies that they are already known. Figures 7 and 8 show a MISFET structure and the corresponding model parameters and disclose no new art. Figures 9 and 10 further show "a method which uses a model generally known as a corner model", implying the corner model is previously known in the art. Figure 11 shows the "conventional" method of determining a device parameter set, "conventional" implying a common method. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. **Claims 1-9** are rejected under 35 U.S.C. 112 second paragraph for being generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. For example, **Claim 1**, step c, recites "normal equation of the least squares method". The meaning is not clear. In another example, consider **Claim 6**. Lines 18 and 19 of **Claim 6** are unclear and the meaning is unknown.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. **Claims 1-9** have been rejected under 35 U.S.C. 102(b) as being anticipated by Kunikiyo et al (U.S. Patent Number 5,845,105), herein referred to as **Kunikiyo**.

12. As to **Claim 1**, **Kunikiyo** teaches a method of simulation wherein variations in an electrical characteristic of a device constituting a semiconductor integrated circuit are represented in the form of a corner model including at least one corner defining a limit of the variations, said method comprising the steps of:

a. preparing a predetermined value tolerable for the variations in said electrical characteristic **(column 7, lines 35-37)**

b. performing a circuit simulation to determine a device parameter sensitivity which is the derivative of said electrical characteristic with respect to a device parameter indicative of information about said device **(Figure 13, Step 50 and column 8, equation 3)**

c. applying said device parameter sensitivity and said predetermined value of said electrical characteristic to the normal equation of the least squares method to determine variations in said device parameter and said at least one corner **(column 10, lines 59-61 and equation 16)**. It is noted that "minimum" and "least" square method refer to the same method.

13. As to the corner model, **Kunikiyo** teaches a model which shows varying electrical characteristics of a device **(Figure 10)** wherein the numbers in circles represent different process conditions. From this chart, electrical characteristics of a process corner can be determined **(column 2 lines 62-63, column 3, lines 12-15)**. It is noted that this model enables a method for arbitrarily choosing "at least one corner

defining a limit of variations" although it is not in the same form as the corner model disclosed in the specification.

14. At to **Claim 2, Kunikiyo** teaches said device parameter including at least one of a model parameter regarding the shape of the device (example t_{ox}) **(column 6, lines 45-48)** and a process parameter regarding a condition during the steps of manufacturing a semiconductor **(Column 6, lines 36-38 and Figure 11)**.

15. As to **Claim 3, Kunikiyo** teaches calculating the variations in said electrical characteristic as said at least one corner **(column 7, lines 50-53)**, based on the multiplication of said device parameter sensitivity and the variations in said device parameter **(column 9, equation 7 and column 10 equation 14)**.

16. As to **Claim 4, Kunikiyo** teaches comparing variations in an electrical characteristic (W_s) and a predetermined value ($W_s$max, $W_s$min) and if the error of said electrical characteristic is greater than the predetermined value, the steps are executed again by fixing a new value for the electrical characteristic and repeating all calculations **(Column 11, equations 16 and 17 and lines 27-38)**. It is noted that changing the value of W_s will further include the steps of determining the device sensitivity parameter, applying this and the predetermined value of the electrical characteristic to the least squares method and calculating the variations in the electrical characteristic since the combination of these steps result in the matrix elements included in equation 16.

17. As to **Claim 5, Kunikiyo** teaches adding a new device parameter and executing the steps of determining the device sensitivity parameter, applying this and the predetermined value of the electrical characteristic to the least squares method and calculating the variations in the electrical characteristic using the new device parameter and said device parameter in combination **(Column 7, 50-63)**.

18. As to **Claim 6, Kunikiyo** teaches said device parameter including a plurality of device parameters **(column 6 lines 35-48)**. **Kunikiyo** further teaches the step of applying device parameter sensitivities and said predetermined values of said electrical characteristics to the normal equation of the least squares method, eliminating a parameter, W_s, and executing on only the remainder of device parameters **(column 11, lines 29-33 and equation 17)**.

19. As to **Claim 7, Kunikiyo** teaches the variations in said device parameters are determined using the weighted least squares method **(column 10, lines 59-61 and equation 16)**. It is noted that because the electrical characteristics and further the device parameter sensitivity were calculated using a weight parameter **(column 7, equation 2 and lines 59-60)**, the method taught by **Kunikiyo** is a weighted least squares method.

20. As to **Claims 8 and 9, Kunikiyo** teaches data input means, data output means, a simulator, data processing means, and a data storage section where the function of extracting parameters is accomplished by a program which runs on the system **(Figure 14, item 72 and column 11, lines 41-43)**. The system in Figure 14 (EWS) shows a display and CPU which is used for data input since it is taught that electrical characteristics as set in the specification must be set. Data output means are shown as the display and the online or satellite communications. A simulator is the program that is run by the EWS and the processing means are accomplished by the CPU. The data storage section for storing data is the memory 72.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C Hogan whose telephone number is 703-305-7838. The examiner can normally be reached on 7:30AM-5PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary C Hogan
Examiner
Art Unit 2123

***

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100